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09/816,933	03/23/2001	Christian Siemers	GR 98 P 8110 P	6157

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EXAMINER	
SIDDIQI, MOHAMMAD A	
ART UNIT	PAPER NUMBER
2154	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/816,933	SIEMERS, CHRISTIAN	
	Examiner	Art Unit	
	Mohammad A. Siddiqi	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *39-76* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1- 38 are presented for examination. Claims 39-76 have been withdrawn from examination. Claims 77-78 have been cancelled.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1 and 20, the phrase "configured in the **same ways** that" renders the claim(s) indefinite because the list of potential alternatives rendering indefiniteness and ambiguity. See MPEP 2100.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-7, 10-11, 13-26, 29-30, 32-38, are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore et al. (6,598,148) (hereinafter Moore) in view of Muthujumaraswathy et al. (6,279,045) (hereinafter Muthujumaraswathy).

6. As per claims 1 and 20, Moore discloses a program-controlled unit (see abstract), comprising: an intelligent core configured to process instructions to be executed (fig 1-8, abstract, col 4, lines 1-30);

a plurality of units selected from the group consisting of internal peripheral units disposed inside the program-controlled unit (fig 1-8, abstract, col 4, lines 1-30), external peripheral units exterior to the program-controlled unit (fig 1-8, abstract, col 4, col 6, lines 26-48, lines 1-30, col 8, lines 1-47), and one or more memory devices (fig 1-8, abstract, col 4, lines 1-45, col 6, lines 26-48, lines 1-30, col 8, lines 1-61); and

an application-specifically configurable intelligent interface (col 14, lines 62-67 and col 15, lines 1-20), for respectively connecting said intelligent core (fig 1-8, abstract, col 13, lines 1-10) and said plurality of units (fig 1-8, abstract, col 13, lines 1-10, col 4, col 6, lines 26-48, lines 1-30, col 8, lines 1-61), including at least one of an interface (external 32 bit bus, col 9, lines 35-41) connection between said intelligent core and said

internal peripheral units (fig 1-8, abstract, col 4, lines 1-30), an interface connection (external 32 bit bus, col 9, lines 35-41) between said intelligent core and said external peripheral units (fig 1-8, abstract, col 13, lines 1-10, col 4, col 6, lines 26-48, lines 1-30, col 8, lines 1-61), an interface connection (external 32 bit bus, col 9, lines 35-41) between said intelligent core and said memory devices (fig 1-8, abstract, col 13, lines 1-10, col 4, col 6, lines 26-48, lines 1-30, col 8, lines 1-61), and an interface connection (external 32 bit bus, col 9, lines 35-41) between said plurality of units (fig 1-8, abstract, col 13, lines 1-10, col 4, col 6, lines 26-48, lines 1-30, col 8, lines 1-61);

said application-specifically configurable intelligent interface including a structurable hardware unit (interface port, 423, fig 17) including at least one of structurable data paths and structurable logic elements (data bus, fig 4, col 4, lines 1-11; col 14, lines 62-67 and col 15, lines 1-20); and said structurable hardware unit (abstract, fig 1-8, col 4, lines 1-11) being configured in the same ways that field-programmable logic arrangements (lines 50-67; col 11, lines 16-36, col 7). Moore explicitly does not disclose hardware unit being configured like a configuration of field-programmable logic arrangements including PLAs, GLAs, PLDs, or FPGAs are configured and to evaluate and process data and/or signal received. However, Muthujumaraswathy discloses said application-specifically configurable

intelligent interface including a structurable hardware unit including at least one of structurable data paths and structurable logic elements (fig 2, col 4, lines 49-67, col 7, lines 32-60); and hardware unit being configured like a configuration of field-programmable logic arrangements including PLAs, GLAs, PLDs, or FPGAs and to evaluate and process data and/or signal received (fig 2, col 4, lines 49-67, col 7, lines 32-60). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Muthujumaraswathy and Moore. The motivation would have been to provide multimedia subsystem on a single IC chip.

7. As per claims 2 and 21, claims are rejected for the same reasons as claim 1, above. In addition, Moore discloses the structurable hardware unit is disposed in circuit terms between said intelligent core and said plurality of units (fig 1-8, abstract, col 13, lines 1-10, col 4, col 6, lines 26-48, lines 1-30, col 8, lines 1-61).

8. As per claims 3 and 22, claims are rejected for the same reasons as claim 1, above. In addition, Moore discloses the structurable hardware unit is connected to a multiplicity of data and signal sources and data and signal destinations (fig 4, col 21-32), and wherein a plurality of multiplexers are

connected to said structurable hardware unit for selecting current data and signal sources and current data and signal destinations (fig 4 and 12, col 4, lines 21-32).

9. As per claims 4 and 23, claims are rejected for the same reasons as claim 1, above. In addition, Moore discloses the data and signal sources and the data and signal destinations comprise units selected from the group of units consisting of said intelligent core, said peripheral units, said memory devices and portions of said structurable hardware unit (fig 1-12, abstract, col 4, lines 21-32, col 12, lines 6-45).

10. As per claims 5 and 24, claims are rejected for the same reasons as claim 1, above. In addition, Moore discloses a structuring of said structurable hardware unit selectively results in an alteration of given data paths and in a configuration of logic elements (idle, col 5, lines 15-20).

11. As per claims 6 and 25, claims are rejected for the same reasons as claim 1, above. In addition, Moore discloses a said structurable hardware unit includes a clock generation unit generating a clock signal and a logic block unit connected to receive the clock signal (col 8, lines 1-5, col 14, lines 37-38), said logic block unit enables devices to be connected via said

structurable hardware unit to cooperate as desired (fig 1-8, abstract, col 13, lines 1-10, col 4, col 6, lines 26-48, lines 1-30, col 8, lines 1-61).

12. As per claims 7 and 26, claims are rejected for the same reasons as claim 1, above. In addition, Moore discloses the clock generation unit and said logic block unit each contain configurable elements (col 8, lines 1-5, col 14, lines 37-38).

13. As per claims 10 and 29, claims are rejected for the same reasons as claim 1, above. In addition, Moore discloses the logic block unit comprises at least one logic block subdivided at least partly into individually configurable sub-blocks with predetermined tasks (abstract, fig 1-12, col 9, lines 51-53, col 10, lines 1-10).

14. As per claims 11 and 30, claims are rejected for the same reasons as claim 1, above. In addition, Moore discloses one of sub-blocks is configured as a processing device enabled for one of arithmetic and logical processing of data input to said sub-block (col 4, lines 1-11).

15. As per claims 13 and 32, claims are rejected for the same reasons as claim 1, above. In addition, Moore discloses one of sub-blocks is configured

as an address calculation device for calculating source and destination addresses (fig 1-8, abstract, col 13, lines 1-10, col 4, col 6, lines 26-48, lines 1-30, col 8, lines 1-61).

16. As per claims 14 and 33, claims are rejected for the same reasons as claim 1, above. In addition, Moore discloses one of sub-blocks is configured as an instruction injection device for injecting instructions into an instruction pipeline of said intelligent core (col 17, lines 15-47).

17. As per claims 15 and 34, claims are rejected for the same reasons as claim 1, above. In addition, Moore discloses the structurable hardware unit is configurable with devices selected from the group consisting of fuses and anti-fuses (fig 6, EPROM).

18. As per claims 16 and 35, claims are rejected for the same reasons as claim 1, above. In addition, Moore discloses the structurable hardware unit is reversibly configurable (abstract, col 17, lines 2-5,).

19. As per claims 17 and 36, claims are rejected for the same reasons as claim 1, above. In addition, Moore discloses the structurable hardware unit is configurable based on data representing a desired configuration, and the data are stored in memory devices insertible into a memory or I/O area

which is addressible by said intelligent core (fig 1-8, abstract, col 4, lines 1-61).

20. As per claims 18 and 37, claims are rejected for the same reasons as claim 1, above. In addition, Moore discloses a configuration of structurable hardware unit is enabled only at predetermined times (fig 1-8, abstract, col 4, lines 1-61).

21. As per claims 19 and 38, claims are rejected for the same reasons as claim 1, above. In addition, Moore discloses the program-controlled configuration of structurable hardware unit is enabled at any time (fig 1-8, abstract, col 4, lines 1-61).

22. Claims 8, 9, 12, 27, 28, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore et al. (6,598,148) (hereinafter Moore) in view of Muthujumaraswathy et al. (6,279,045) (hereinafter Muthujumaraswathy) as applied to claims 1 and 20 above, and further in view of Takahashi et al. (5,825,878) (hereinafter Takahashi).

23. As per claims 8 and 27, Moore discloses the clock generation unit is formed at least in part by a device selected from the group consisting of a DNF logic configuration, an array, a multiplexer-based logic variant, and a

structurable logic configuration (fig 4 and 12, col 29, lines 30-50, col 12, lines 19-40). Moore and Muthujumaraswathy are silent about NAND. However, Takahashi discloses NAND (fig 6, col 10, lines 36-38). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine Takahashi with Moore and Muthujumaraswathy. The Motivation would have been to provide a high performance microprocessor that can be directly connected to memory controller.

24. As per claims 9 and 28, the claim is rejected for same reasons as claim 8, above. in addition, Takahashi discloses NAND (fig 6, col 10, lines 36-38).

25. As per claims 12 and 31, the claim is rejected for same reasons as claim 8, above. In addition, Takahashi discloses one of sub-blocks is configured as a state machine for central sequence control (fig 4, col 6, lines 52-55).

Response to Arguments

26. Applicant's arguments filed 07/30/2007 have been fully considered but they are not persuasive, therefore rejections to claims 1-38 is maintained.

27. In the remarks applicants argued that:

Argument: Moore does not disclose said application-specifically configurable intelligent interface including a structurable hardware unit including at least one of structurable data paths and structurable logic elements.

Response: Moore discloses said application-specifically configurable intelligent interface (interface port, 423, fig 17) including a structurable hardware unit including at least one of structurable data paths and structurable logic elements (data bus, fig 4, col 4, lines 1-11; col 14, lines 62-67 and col 15, lines 1-20). Muthujumaraswathy discloses said application-specifically configurable intelligent interface including a structurable hardware unit including at least one of structurable data paths and structurable logic elements (fig 2, col 4, lines 49-67, col 7, lines 32-60); and hardware unit being configured like a configuration of field-programmable logic arrangements including PLAs, GLAs, PLDs, or FPGAs and to evaluate and process data and/or signal received (fig 2, col 4, lines 49-67, col 7, lines 32-60). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Muthujumaraswathy and Moore. The motivation would have been to provide multimedia subsystem on a single IC chip.

Conclusion

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohammad A. Siddiqi whose telephone number is (571) 272-3976. The examiner can normally be reached on Monday -Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MAS

NATHAN FLYNN
SUPERVISORY PATENT EXAMINER